What Is Claimed Is

1. A method of implementing the multi-sectional encoding indexing method, whether covering:

   Step 1: An m sectional encoding structure which is comprised of $\overline{A_i}'''$, $i = 0, 1, \ldots, m-1$, each $\overline{A_i}''$ has at most 2^{k_i} varieties.

   Step 2: $\overline{A_i}'''$ can be transferred into $\overline{A_i}''$. Upon transference, $\overline{A_i}'$ will have k_i bits varied, and thus $\sum_{i=0}^{m-1} k_i = n$. n stands for the index bit width of the Indexing Method.

   Step 3: $\overline{A_i}''$ operated with $(2^n - 1)$ by AND bit by bit, can be transferred to $\overline{A_i}'$ of n bit width.

   Step 4: If $\overline{A_i}'$ is transferred into $\overline{A_0} \oplus \overline{A_1} \oplus \ldots \oplus \overline{A_{m-1}}$, then bits of $\overline{A_i}$, from $n - (\sum_{j=0}^{i-1} k_j + 1)$ to $n - \sum_{j=0}^{i} k_j$, will become variable ones. ($\sum_{j=0}^{-1} k_j = 0$ is assumed for short.) $\overline{A_0} \oplus \overline{A_1} \oplus \ldots \oplus \overline{A_{m-1}}$ has a feature that different output values can be produced as long as the values input vary, i.e. having the effect of "collision free."

2. The method of implementing the multi-sectional encoding indexing method, according to the claim 1, two methods are presented and can be applied single or mingled as step 2 required. The purpose of both methods is to minimize the k_i every with a view to shortening the index n bit width, in which, $\sum_{i=0}^{m-1} k_i = n$

3. The method of implementing the multi-sectional encoding indexing method, according to the claim 1, the first method is to observe each $\overline{A_i}'''$, if the variable bits are not at the right side, adjust them.

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4. The method of implementing the multi-sectional encoding indexing method, according to the claim 1, the second method can be applied under the following conditions:

$\min(\overline{A_i}^{\varpi_{''}}) \leq \overline{A_i}^{\varpi_{'''}} \leq \max(\overline{A_i}^{\varpi_{'''}})$, k_i then satisfy the formula:

$2^{k_i-1} < (\max(\overline{A_i}^{\varpi_{'''}}) - \min(\overline{A_i}^{\varpi_{'''}}) + 1) \leq 2^{k_i}$, add or subtract a certain value to or from the

encoding structure value, $\overline{A_i}^{\varpi_{''}}$, converting it into whose k_i bits are

variable. A particular value for subtraction is $\min(\overline{A_i}^{\varpi_{'''}})$.

5. An implementation method of the reverse compensation indexing method, whether covering:

Step 1: The two-sectional encoding structure is comprised of $\overline{A_i}^{\varpi_{''}}$ $i = 0,1$, and

the value of each encoding structure is $\min(\overline{A_i}^{\varpi_{''}}) \leq \overline{A_i}^{\varpi_{'''}} \leq \max(\overline{A_i}^{\varpi_{'''}})$:

k_i in which satisfy the following formula:

$2^{k_i-1} < (\max(\overline{A_i}^{\varpi_{'''}}) - \min(\overline{A_i}^{\varpi_{'''}}) + 1) \leq 2^{k_i}$

Step 2: After adding or subtracting a certain value to or from $\overline{A_i}^{\varpi_{''}}$, k_0 bits

of $\overline{A_0}^{\varpi_{''}}$ and k_1 bits of $\overline{A_1}^{\varpi_{''}}$ may be change, and $\sum_{i=0}^{1} k_i = n$, in

which n is the width of the index bits.

Step 3: $\overline{A_i}^{\varpi_{''}}$, operated with $(2^n - 1)$ by AND bit by bit, is transferred to $\overline{A_i}^{\varpi}$

of n bits;

Step 4: $\overline{A_0}^{\varpi}$, obtained by reversing the bit locations of $\overline{A_0}^{\varpi_{'}}$, is operated with

$\overline{A_1}^{\varpi}(=\overline{A_1}^{\varpi_{'}})$ by exclusive-OR, i.e., $\overline{A_0}^{\varpi} \oplus \overline{A_1}^{\varpi}$; The feature is that the

output values produced by the indexing method will be different if

input of different values, i.e. having the effect of "collision free."

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6. The method of implementing the multi-sectional encoding indexing method, according to the claim 5, the outstanding property of the reverse compensation indexing method to be illustrated: if min(VPI) =0 and min(VCI) =0, then this single circuit can be applied in

$$\frac{\max(VPI) = 2^{k_0} - 1}{\max(VCI) = 2^{n-k_0} - 1}, k_0 = 0,1,...,n$$

up to (n+1) occasions, all of which have the effect of "collision free."

7. A method that corresponds multi-sectional encoding structures to a single indexing table is presented. The receiving unit of the ATM can support different VPI/VCI connection amounts by relatively adding or subtracting the Indexing Table Memory equipped in the said unit, in coordination with the TBWA circuit. The input exclusive-OR configuration of VPI and VCI may be changed according to the bit width of the indexing table Memory.

8. A structure is presented that corresponds multi-sectional encoding structures to shared memories. The Indexing Table Memory of e entries, from Entry 0 to e-1, i.e. Entry 0, Entry 1, ...to Entry e-1. $\sum_{i=0}^{r-1} 2^{TBW_i} = e$, then the base pointer of the input unit 0 is BP_0, and those of the base pointer for other r-1 input ports is figured out by the TBW and BP of the previous unit. Its formula is $BP_i = BP_{i-1} + W * 2^{TBW_{i-1}}, i = 1,...,r-1$. The purpose of calculating every BP is to orderly and compatibly allocate every section of the indexing table memory used by different input ports. Such kind of the shared memory structure can more effectively adjust the connection amount of every input port with limited indexing table memory.

9. An applied method of multi-sectional encoding structures whether divided into sets of two sections and every set is regarded as a basic unit for implementing the reverse compensation indexing method. Therefore, this

kind of multi-sectional encoding structures may have the same flexibility necessary for application of the reverse compensation indexing method.